

## **ABSTRACT**

A method for predicting processor inactivity for a controlled transition of power states. The method of one embodiment comprises predicting a first event that allows for lower performance in a processor. The processor is transitioned from a high performance state to a low performance state upon prediction of the first event. A second event that can utilize greater performance in the processor is detected. The processor is transitioned from the low performance state to the high performance state upon detection of the second event.